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| EXAMINER | |
|---|---|
| MITCHELL, JASON D | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/585,680 | JIANG ET AL. | |
| | Examiner | Art Unit | |
| | JASON MITCHELL | 2193 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/11/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This action is in response to an application filed on 7/10/06.

Claims 1-20 are pending in this application.

### *Specification*

**The disclosure is objected to because of the following informalities:**

In par. [0074] the applicants refer to "the second memory access chain 2->6->12". The examiner does not understand how this memory access chain was derived. Specifically it is noted that no direct dependency exists between nodes 6 and 12 (see e.g. Fig. 8), thus it is believed the disclosed 'memory access chain ... 6->12' is inconsistent with the rest of the disclosure.

Appropriate clarification or correction is required.

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

**Claims 13-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.**

**Claim 13** is not limited to statutory embodiments. In view of Applicant's disclosure, specification page 18, par. [0090], the claimed medium is not limited to statutory embodiments, instead being defined as including both statutory embodiments (e.g., "any medium that is capable of storing ... instructions for execution"; presumably

the exemplary "floppy diskettes, optical disks, CD-ROMs, and magneto-optical disks") and non-statutory embodiments (e.g., "any medium that is capable of ... encoding a sequence of instructions for execution"; this would include communication media such as wireless signals). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

**Claims 14-15** depend from claim 13 and are rejected accordingly.

**Claim 16** fails to fall within a statutory category of invention. It is directed to a program itself (i.e. "A code partitioning unit, comprising: a dependence information [software] unit ... ; and a code partitioning [software] unit"), not a process occurring as a result of executing the program, a machine programmed to operate in accordance with the program or a manufacture structurally and functionally interconnected with the program in a manner which enables the program to act as a computer component and realize its functionality. It's also clearly not directed to a composition of matter. Therefor it is rejected as being non-statutory under 35 USC 101.

**Claims 17-20** depend from claim 16 and are rejected accordingly.

***Claim Objections***

**Claims 4, 6, 15, 17 and 19 are objected to because of the following informalities:**

**Claim 4** recites "assigning instructions in the code for which the first number of desired upstream nodes are dependent on to the upstream stage". It is believed this would more properly read "assigning instructions in the code ~~for~~ on which the first number of desired upstream nodes are dependent ~~on~~ to the upstream stage".

**Claims 6, 15, 17 and 19** make similar recitations and are objected to according.

**Claim 14** recites "instructions which when executed causes the machine to". It is believed this would more properly read "instructions which when executed ~~causes~~ cause the machine to".

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**Claims 6 and 17-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.** The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

**Claim 6** recites "if a compute weight of the upstream stage exceeds a predetermined value". While the specification refers repeatedly to a "compute weight" nowhere do the applicants disclose what a "compute weight" is or, more importantly, how it would be calculated. Further, the term "compute weight" does not appear to be a term used in the relevant arts. Accordingly those of ordinary skill in the art would not

have been enabled to calculate a "compute weight of the upstream stage" in accordance with the applicants disclosed embodiments without undue experimentation.

**Claims 17-19** make similar reference to a "compute weight" and are rejected accordingly.

**Claim 20** depends on claim 19 and is rejected accordingly.

**Claim 8 and 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

**Claim 8** recites the limitation "instruction in the code which are dependent on the first number of desired downstream nodes" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim. It is believed the claim would more properly read "instruction in the code which are dependent on the ~~first~~ last number of desired downstream nodes".

**Claim 16** recites "A code partitioning unit, comprising: ... a code partitioning unit". The use of the term "code partitioning unit" to refer to two apparently distinct units raises questions of clarity. It is suggested that the claim be amended to rename one or the other of these units.

**Claim 17** recites "a length unit to determine a number of desired lengths of upstream nodes". It is not clear what is intended by "a number of desired lengths". The examiner assumes this language is intended to describe "a length unit" with determines

a desired number of upstream nodes or alternately a 'length' of the upstream partition (e.g. a number of nodes the system will place in the 'upstream' partition).

Further, claim 17 recites "an assignment unit to assign a first number of desired length of upstream nodes to the upstream stage". In addition to the lack of clarity described above, it is not clear from this language if this recitation of "a first number ..." is intended to refer to the "first number ..." recited in line 2, or a second distinct "first number ...". For the purposes of this examination the former understanding will be used.

**Claim 18** recites "the evaluation unit ... the compute weight ... [and] the predetermined value" in lines 2-3. There is insufficient antecedent basis for these limitations in the claim. The examiner notes that claim 17 provides sufficient antecedent basis for these claims. Accordingly, for the purposes of this examination claim 18 will be treated as dependant on claim 17.

**Claim 19** recites limitations similar to those discussed in conjunction with claim 17 (i.e. "determines a number of desired length of downstream nodes"; "assigns a first number of desired length") and is rejected accordingly.

**Claim 20** depends on claim 19 (which in turn depends on claim 16) and is rejected accordingly.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claim 1-4, 7-8 and 10-16 are rejected under 35 U.S.C. 102(b) as being anticipated by "Partitioning a Lenient Parallel Language into Sequential Threads" by Ha, Han and Kim.**

**Claims 1 and 13:** Ha discloses a method of compiling code, comprising:

partitioning instructions in the code among a plurality of processors based on memory access latency associated with the instructions (pg. 85, col. 2, Section 4 "DAVRID graphs are first partitioned based on only long latency instructions").

**Claim 2:** The rejection of claim 1 is incorporated; further Ha discloses partitioning instructions comprises partitioning memory access dependence chains (pg. 85, col. 2, Section 4.1 2nd par. "We partition the DAVRID graphs by … using dependence set").

**Claim 3:** The rejection of claim 1 is incorporated; further Ha discloses partitioning instructions comprises partitioning a memory access dependence chain into an upstream stage (pg. 85, col. 2, Section 4.1 2nd par. "We partition the DAVRID graphs by … using dependence set"; because the term 'upstream' is at best loosely defined in the specification, it appears that any first partition will meet this claim limitation).

**Claims 4 and 15:** The rejections of claims 1 and 13 are incorporated; further Ha discloses partitioning instructions comprises partitioning a memory access dependence

chain into an upstream stage by assigning a first number of desired upstream nodes to the upstream stage, and assigning instructions in the code for which the first number of desired upstream nodes are dependent on to the upstream stage (pg. 85, col. 2, Section 4.1, 2nd par. "We partition the DAVRID graphs by cutting remote arcs logically ... using dependence set developed by Iannucci[4]").

**Claim 7:** The rejection of claim 3 is incorporated; further Ha discloses partitioning the memory access dependence chain into a downstream stage (pg. 85, col. 2, Section 4.1 2nd par. "We partition the DAVRID graphs by ... using dependence set"; again because the term 'downstream' is, at best, loosely defined in the specification, it appears that any second or subsequent partition will meet this claim limitation).

**Claim 8:** The rejection of claim 7 is incorporated; further Ha discloses partitioning the memory access dependence chain into the downstream stage comprises:

assigning a last number of desired downstream nodes to the downstream stage (pg. 85, col. 2, Section 4.1, 2nd par. "We partition the DAVRID graphs by cutting remote arcs logically"); and

assigning instructions in the code which are dependent on the first number of desired downstream nodes to the downstream stage (pg. 85, col. 2, Section 4.1, 2nd par. "We partition the DAVRID graphs by ... using dependence set developed by Iannucci[4]").

**Claim 10:** The rejection of claim 1 is incorporated; further Ha discloses identifying instruction dependence information (pg. 85, col. 2, Section 4.1, 2nd par. "dependence set developed by Iannucci[4]").

**Claims 11 and 14:** The rejections of claims 1 and 13 are incorporated; further Ha discloses constructing a memory access dependence graph (pg. 85, col. 2, Section 4.1, 2nd par. "dependence set developed by Iannucci[4]").

**Claim 12:** The rejection of claim 1 is incorporated; further Ha discloses:

constructing a memory access dependence graph (pg. 85, col. 2, Section 4.1, 2nd par. "dependence set developed by Iannucci[4]"); and

identifying a memory access dependence chain from the memory access dependence graph (pg. 85, col. 2, Section 4.1, 2nd par. "We partition the DAVRID graphs by ... using dependence set developed by Iannucci[4]").

**Claim 16:** Ha discloses a code partitioning unit, comprising:

a dependence information unit to identify dependencies between instructions in code (pg. 85, col. 2, Section 4.1, 2nd par. "We partition the DAVRID graphs by ... using dependence set developed by Iannucci[4]"); and

a code partitioning unit to partition instructions in the code among a plurality of processors based on memory access latency associated with the instructions (pg. 85,

col. 2, Section 4.1, 2nd par. "We partition the DAVRID graphs by cutting remote arcs logically").

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Partitioning a Lenient Parallel Language into Sequential Threads" by Ha, Han and Kim in view of US 5,768,594 to Blelloch et al.**

**Claim 5:** The rejection of claim 4 is incorporated; further Ha does not disclose the number of desired upstream nodes is the length of the memory access dependence chain divided by a pipelining degree.

Blelloch teaches partitioning code such that the number of desired upstream nodes is the length of the memory access dependence chain divided by a pipelining degree (col. 4, lines 19-22 "In step 610, the assignment manager AM1 partitions the N selected tasks to p groups of size approx (N/p) each, where p is the number of available processing elements PE1").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to partition Ha's selected tasks (Ha pg. 85, col. 2, Section 4 "first partitioned based on only long latency instructions"; pg. 85, col. 2, Section 4.1, 2nd par. "using dependence set developed by Iannucci[4]") such that the number of desired upstream nodes is the length of the memory access dependence chain (Ha pg. 85, col. 2, Section 4.1, 2nd par. "using dependence set developed by Iannucci[4]"; Blelloch col. 4, lines 19-22 " the N selected tasks ... (N/p)") divided by a pipelining degree (Blelloch col. 4, lines 19-22 " (N/p) ... where p is the number of available processing elements PE1"). Those of ordinary skill in the art would have been motivated to do so as a known method for partitioning the instructions (Blelloch col. 4, lines 19-22 "partitions the N selected tasks") which would have provided the disclosed load balancing (Ha pg. 84, col. 2, 1st par. "The message handling unit ... manages ... load balancing").

**Claim 9:** The rejection of claim 8 is incorporated; further Ha does not disclose the number of desired downstream nodes is N*(d- 1)/d, where N is a length of the memory access dependence chain, and d is a pipelining degree.

Blelloch teaches partitioning code such that the number of desired downstream nodes is N*(d- 1)/d, where N is a length of the memory access dependence chain, and d is a pipelining degree (col. 4, lines 19-22 "In step 610, the assignment manager AM1 partitions the N selected tasks to p groups of size approx (N/p) each, where p is the number of available processing elements PE1"). Note that in a two processor system

Blelloch's partition sized is as claimed (i.e. N*(2-1)/2 = N/2). Further, in a system with more than two processors the second and subsequent partitions can be considered the 'downstream' partition resulting in the claimed partition size (i.e. N*(d-1)/d = N/p*(p-1), where d=p). This understanding appears to match the disclosed process where the downstream partition is itself recursively partitioned into upstream and downstream partitions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to partition Ha's selected tasks (Ha pg. 85, col. 2, Section 4 "first partitioned based on only long latency instructions"; pg. 85, col. 2, Section 4.1, 2nd par. "using dependence set developed by Iannucci[4]") such that the number of desired downstream nodes is the length of the memory access dependence chain (Ha pg. 85, col. 2, Section 4.1, 2nd par. "using dependence set developed by Iannucci[4]"; Blelloch col. 4, lines 19-22 " the N selected tasks ... (N/p)") divided by a pipelining degree (Blelloch col. 4, lines 19-22 " (N/p) ... where p is the number of available processing elements PE1") resulting in a downstream partition as claimed. Those of ordinary skill in the art would have been motivated to do so as a known method for partitioning the instructions (Blelloch col. 4, lines 19-22 "partitions the N selected tasks") which would have provided the disclosed load balancing (Ha pg. 84, col. 2, 1st par. "The message handling unit ... manages ... load balancing").

***Examiner's Comment***

The lack of a prior art rejection for claims 6 and 17-20 should not necessarily be taken as an indication of patentable subject matter. Further search and consideration will be required upon correction of the clarity issues (see e.g. 35 USC 112 1st rejections above). Further, depending on the nature of the response, any resulting rejection may or may not constitute a new ground of rejection requiring a non-final action.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON MITCHELL whose telephone number is (571)272-3728. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bullock Lewis can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason Mitchell/
Examiner, Art Unit 2193